AFB
IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: DIETMAR EGGERT WOLFRAM KLUGE	Group Art Unit: 2836
	Examiner: KIM NGOC HUYNH
Serial No.: 09/468,015	Conf. No.: 3122
Filed: DECEMBER 20, 1999	Atty. Dkt.: 2000.065900/DE0005 (formerly F71989US)
For: ELECTROSTATIC DISCHARGE PROTECTION NETWORK HAVING DISTRIBUTED COMPONENTS	CUSTOMER NO.: 23720

APPEAL BRIEF

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8	
DATE OF DEPOSIT:	June 1, 2005
I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as "FIRST CLASS MAIL" addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Signature	

MAIL STOP APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On April 4, 2005, Appellants filed a Notice of Appeal in response to a Final Office Action dated December 3, 2004, issued in connection with the above-identified application. In support of the Appeal, Appellants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences.

Since the Notice of Appeal for the present invention was received and stamped by the USPTO Mailroom on April 11, 2005, the two-month date for filing this Appeal Brief is June 11, 2005. This Appeal Brief is being filed on June 1, 2005, thus, this paper is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

The Commissioner is authorized to deduct the fee for filing this Appeal Brief ($500.00) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0005. No additional fees are believed to be due. However, should any additional fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Commissioner is authorized to deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0005.[1]

I. REAL PARTY IN INTEREST

The prosecution history reveals that the present patent application was initially assigned to Advanced Micro Devices, Inc. ("AMD") and the real party in interest is AMD.

II. RELATED APPEALS AND INTERFERENCES

Appellants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-24 are pending in the application.

[1] In the event the monies in that account are insufficient, the Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.065900.

Claims 1-3 stand rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,969,929 (***Kleveland***). Claims 1-20 stand rejected as being unpatentable under 35 U.S.C. § 103(a) as being obvious over ***Kleveland*** in view of U.S. Patent No. 5,576,680 (***Ling***). The claims currently under consideration, *i.e.*, claims 1-24, are attached as Appendix A.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF THE INVENTION

Appellants' inventive methodologies are generally directed to electronic circuits and systems sensitive to electrostatic discharge, and more particularly, to a distributed electrostatic discharge protection network for these electronic circuits and systems operating at radio frequencies. *See,* p. 1, ll. 6-8.

The present invention provides a system, method and apparatus for providing an electrostatic discharge protection network on an integrated circuit die, a monolithic substrate, and a printed circuit board with or without constant impedance stripline conductors. Various embodiments of the invention include an inductor that has at least one or more turns of a coil, and one or more ESD clamp device connected to the coil(s). More than one coil turn may be associated with one ESD clamp device, and more than one ESD clamp device may be associated with one turn of the coil. The inductor coil may be comprised of any shape or form, and the ESD clamp device may be any other type of transient voltage limiting device. *See,* p. 3, ll. 5-15.

The inductor portion may be connected in series between an electronic circuit node that is being protected, and an external signal node, which is subject to an ESD event. The ESD clamp device(s) may be connected to the inductor, preferably at each turn of the inductor coil, and to one or both of the common power supply rails. One of the common power supply rails may be at earth ground potential. In addition, it is contemplated and within the scope of the present invention that some of the ESD clamp devices may also be connected between one or more turns of the inductor coil and earth ground. *See*, p. 3, ll. 16-23.

Figure 2 illustrates a schematic diagram of the ESD protection circuit of the embodiments of the invention. The ESD protection circuit 200 has an external node 206 and an internal node 208. The external node 206 is adapted for connection to circuits having desired signals with undesirable ESD events and the internal node 208 is adapted for connection to circuits needing protection from ESD events. Between the nodes 206 and 208, the ESD protection circuit 200 comprises a series connected inductor 202 between the nodes 206 and 208, wherein the inductor 202 has tapped portions (202a, 202b, 202c and 202d). Parallel or shunt connected ESD clamp devices represented by their parasitic capacitance (204a, 204b, 202c and 204d) are connected to respective inductor 202 tapped portions (202a, 202b, 202c and 202d). The inductor 202 and ESD clamp parasitic capacitance 204 form cascaded "n" sections of a low pass filter network. The series inductance of the inductor coil 202 portions (202a, 202b, 202c and 202d) preferably cancel out the shunt parasitic capacitance (204a, 204b, 202c and 204d) of the ESD clamp device(s) connected thereto for signal frequencies below the low pass filter cutoff frequency. Appropriate selection of inductance 202 and capacitance 204 values for the ESD network 200

may also be used for efficient impedance matching of the signal nodes 206 and 208 to a source and load, respectively. *See,* p. 10, ll. 1-17.

Figure 3 illustrates a schematic orthogonal view of an embodiment of the invention. The inductor 202 may include one or more turns formed from conductive layers that are coil shaped. These coil shaped conductive layers, (coil turns 202a, 202b, 202c, 202d) are formed on a plurality of insulation layers. Each coil shaped conductive layer is formed on a respective insulation layer (See Figure 4). Various "vias" through the insulation layers are used to connect the different coil shaped conductive layers together by conductive connections. The shape of the coil may vary, for example, the shape may be round, square, rectangle, triangle, oval, hexagon, octagon and the like. The conductive layer may be made from one or more various metals, such as copper, aluminum, copper alloy and aluminum alloy, or any other conductive material used in the fabrication of an integrated circuit, such as conductive doped polysilicon. *See,* p. 10, l. 18, through p. 11, l 7.

Figure 4 illustrates a cross-section view of the fabricated ESD network 200. An integrated 10 circuit die 400 includes a substrate 410 that contains various doped wells (412a, 412b, 412c and 412d), in which ESD clamp devices have either or both PMOS and NMOS transistors. The PMOS and NMOS transistors of the ESD clamp devices may be connected to the power supply rails, V_{DD} and Vss'. *See,* p. 11, ll. 8-13.

Insulation layer 414d is formed over the substrate 410 and wells (412a, 412b, 412c, 412d). The insulation layer 414d may also be formed over other conducting and insulation

layers proximate to the substrate 410. The coil turn 202d is formed over the insulation layer 414d. Similarly, other insulation layers (414c, 414b, 414a) and coil turns (202c, 202b, 202a) are formed as illustrated in Figure 4. Another insulation layer 416 may be formed over the 20 coil turn 202a for additional circuitry or physical protection of the integrated circuit die. *See,* p. 11, ll. 15-20.

The ESD clamp devices formed in the wells (412a, 412b, 412c, 412d) may be connected to the coil turns (202a, 202b, 202c, 202d) respectively, through conductive vias (holes) in the insulation layers (414a, 414b, 414c, 414d). The vias are filled with a conductive material such as aluminum. As illustrated in Figure 4, vias 418a pass through insulation layers (414d, 414c, 414b), and connect the ESD clamp device in the well 412a to the coil turn 202a. The vias 418a do not connect to the other coil turns 202b, 202c and 202d. Vias 418b pass through insulation layers 414d, 414c and 414b, and connect the ESD clamp device in the well 412b to the coil turn 202b. The vias 418b do not connect to the other coil turns (202a, 202c, 202d). Vias 418c pass through insulation layers 414d and 414c, and connect the ESD clamp device in the well 412c to the coil turn 202c. The vias 418c do not connect to the other coil turns (202a, 202b, 202d). Via 418d passes through insulation layer 414d, and connects the ESD clamp device in the well 412d to the coil turn 202d. The internal node 208 connects to circuit logic (not illustrated) of the integrated circuit die, and the external node 206 is adapted for connection to external circuitry. It is also contemplated and within the scope of the invention that the ESD clamp devices may be formed on or attached to each of the insulation layers. *See,* p. 11, l. 21 through p. 12, l. 13.

According to another embodiment of the invention, the ESD protection network 15 may be fabricated on a substrate made of either insulation material (*e.g.*, ceramic, glass epoxy, a printed wiring board (PWB), *etc.*), or conductive material (*e.g.*, aluminum, copper, steel brass, *etc.*). A plurality of turns of a coil are formed on a plurality of insulation layers on the substrate. Each one of the insulation layers has one of the coil turns. Vias are formed in each of the plurality of insulation layers, and conductive material is deposited therein for connecting the plurality of coil turns together to form the inductor. The ESD clamp devices may be formed or attached on each of the insulation layers or the ESD clamp devices may be attached to the substrate with connection to the plurality of coil turns made through conductive vias in the various insulation layers on which the coil turns are formed. *See,* p. 12, ll. 14-24.

Figure 5 illustrates a schematic elevational cross-section view of the ESD network fabricated on a substrate. A substrate 510 may be non-conductive or conductive. If the substrate is conductive, an insulation layer 516 may be used. If the substrate is non-conductive then no insulation layer 516 may be required. A first coil turn 202a is formed over the insulation layer 516 or over the non-conductive substrate 510. The first coil turn 202a is connected to an external input node 206. An insulation layer 514a is formed over the first coil turn 202a. A second coil turn 202b is formed over the insulation layer 514a. Another insulation layer 514b is formed over the second coil turn 202b. A third coil turn 202c is formed over the insulation layer 514b. Still another insulation layer 514c is formed over the third coil turn 10 202c. Yet another insulation layer 514d is formed over the third coil turn 202c. A fourth coil turn 202d is formed over the insulation layer 514c. And another insulation layer 514d is formed over the fourth coil turn 202d. The fourth coil turn 202d is connected to an internal node 208. Any number of coil turns

and insulation layers are contemplated and within the scope of the present invention. *See,* p. 13, ll. 1-14.

ESD clamp devices (512a, 512b, 512c, 512d) may comprise PMOS and NMOS transistors, and may be connected to power supply rails, V_{DD} and Vss, in a fashion similar to the PMOS and NMOS transistor connections illustrated in Figure 1. The ESD clamp devices may be any type of clamp device, connected to a substrate common or earth ground. The ESD clamp devices (512a, 512b, 5l2c, 512d) may be connected to the coil turns (202a, 202b, 202c, 202d), respectively, through conductive vias (holes) in the insulation layers (514a, 514b, 514c, 514d). The vias are filled with a conductive material such as aluminum. As illustrated in Figure 5, vias 518a pass through insulation layers (514d, 514c, 514b), and connect the ESD clamp device 512a to the coil turn 202a. The vias 518a do not connect to the other coil turns (202b, 202c, 202d). Vias 518b pass through insulation layers (514d, 514c, 514b), and connect the ESD clamp device 512b to the coil turn 202b. The vias 518b do not connect to the other coil turns (202a, 202c, 202d). Vias 518c pass through insulation layers 514d and 514c, and connect the ESD clamp device 512c to the coil turn 202c. The vias 518c do not connect to the other coil turns 202a, 202b and 202d. Via 518d passes through insulation layer 514d, and connects the ESD clamp device 512d to the coil turn 202d. It is also contemplated and within the scope of the invention, that the ESD clamp devices may be formed on each of the insulation layers and attached to the conductive layer coil turns on the insulation layers. *See,* p. 13, l. 15 through p. 14, l. 8.

Figures 6 and 7 illustrate a schematic plan view and an elevational view, respectively, of an ESD protection network fabricated on a non-conductive printed circuit board using printed

circuit strip line conductors and surface mounted components. The transmission line structures may be used instead of coil shaped structures with the ESD clamp devices. The non-conductive portion of a printed circuit board 610 may be, for example, glass epoxy, TEFLON®, ceramic, glass, *etc.* The printed circuit strip line enables constant impedance for the signal path. A plurality of turns of a coil 602 are formed on the printed circuit board 610 in a concentric spiral configuration. Conductive vias 612a-612d (plated through holes) may be formed through the printed circuit board 610 at each of the plurality of coil turns, or portions thereof. ESD clamp devices 604a-604d may be attached to respective ones of these vias 612a-612d and to a planar ground plane 712. The ground plane 712 may be located on the face opposite the face on which the plurality of coil turns 602 is located thereon. The ESD clamp devices 604 may be connected to the coil turns 602 by vias 612 and to the planar ground plane 710 by vias 608, or, preferably, by using surface mount techniques. The plurality of coil turns 602 may be tapped with, for example, the vias 612 at points along the coil 602, which may represent a desired inductance, needed to cancel out the parasitic capacitance of the associated ESD clamp devices 604. The ESD clamp devices 604 may connect to the outer or larger coil turn(s) at less than 360 degrees, and the inner or smaller coil turns 602 at more than 360 degrees, *i.e.*, a multiple turn. *See,* p. 14, l. 9 through p. 15, l. 5.

The insulation layers between the coil turns of the inductor may preferably be very thin so that the turns of the coil are close together, thus, improving the magnetic coupling therebetween and increasing the effective inductance for a given size coil diameter. Referring to Figure 8, a schematic orthogonal view of the coil portion of Figure 3 and a core having magnetic properties to increase the inductance of the coil 202 is illustrated. A core 820 comprising a

material of high magnetic permeability may be located within the coil 202 to further increase the effective inductance value for a given size of coil structure. This material may be, for example, iron, iron oxide, ferrite ceramic, ferrous oxide, or other materials that increase the effective inductance of the inductor coil. *See,* p. 15, ll. 6-15.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-24 are pending in the application.

Appellants respectfully request that the Board review and overturn the following rejections present in this case. The following grounds of rejections to be reviewed are presented on Appeal in this case:

1. Whether claims 1-3 and 21-24 are anticipated under U.S.C. § 102(a) by U.S. Patent No. 5,969,929 (***Kleveland***).

2. Whether claims 4-20 are obvious under 35 U.S.C. § 103(a) over ***Kleveland*** in view of U.S. Patent No. 5,576,680 (***Ling***).

VII. ARGUMENT

The present invention is directed to a plurality of ESD clamp devices being connected to a corresponding one of a plurality of turns on an inductor, wherein the inductor and the parasitic capacitance is used to form a low pass filter. *See*, Specification, page 8, lines 15-23. The present invention also provides for novel applications of vias to interconnect coil shaped elements to produce an inductive element.

The Examiner relies heavily on ***Kleveland*** to reject the pending claims in the instant patent application. In contrast to the various embodiments of the claimed invention, ***Kleveland*** is directed to reducing parasitic capacitance of the protection circuit to reduce data transmission in high frequency devices and, therefore, does not function as a low pass filter. *See*, col. 5, lines 22-26. In fact, ***Kleveland*** directs one away from the claimed invention. The Examiner also relies on ***Ling*** to compensate for the shortcomings of ***Kleveland***. However, ***Ling*** does not make up for the deficits of ***Kleveland***. ***Ling*** is merely directed to forming an inductive circuit on a semiconductor chip. ***Ling*** provides for patterned lines to form an inductor. Although ***Ling*** discloses a plurality of inductor elements formed on different horizontal planes, ***Ling*** does not disclose the subject matter that is lacking in ***Kleveland,*** but is called for by claims of the present invention. *See* col. 7, lines 59-65. In other words, ***Ling*** does not disclose the element that the Examiner claims is missing from ***Kleveland***, *e.g.*, a via used to connect coil shaped inductive elements to produce an inductive element.

A. **Claims 1-3 and 21-24 Are Not Anticipated Under U.S.C. § 102(a) by U.S. Patent No. 5,969,929 (*Kleveland*).**

Independent claims 1 and 21 of the present invention call for forming a low pass filter using parasitic capacitance and ESD protection elements. In contrast, ***Kleveland*** is directed to reducing capacitance of ESD protection and providing a reduction in the parasitic capacitance in order to maintain the bandwidth of high frequency devices. Therefore, the disclosure of ***Kleveland*** provides for passing high frequency signals. This amounts to a high pass filter, which is the opposite of the low pass filter that is called for by claims 1-3 and 21-24. Therefore, ***Kleveland*** actually directs one away from claims 1 and 21 of the present invention. ***Kleveland*** promotes reducing parasitic capacitance in an attempt to avoid reducing the bandwidth of high frequency devices. Accordingly, ***Kleveland's*** disclosure provides for not reducing high-frequency signals, which is in contrast with the elements of independent claims 1 and 21.

Group I Claims (Claims 1-3 and 21-24) Are Not Anticipated Under U.S.C. § 102(a) By *Kleveland*. Group I claims stand or fall together.

All of the elements of Group I claims (i.e., claims 1-3 and 21-24) are not taught, disclosed, or suggested by ***Kleveland***. In the Advisory Action dated February 23, 2005, the Examiner inadvertently misconstrued Appellants' disclosure in the Specification, which discusses reducing the shunt capacitance of the ESD clamp device. The Examiner mistakenly seized this partial idea to equate it to ***Kleveland's*** disclosure of promoting a reduction in the parasitic capacitance. However, the Examiner inadvertently missed the point in the Specification, which discloses that a reduction in the shunt capacitance of the ESD clamp device is present "...for signal frequencies below the low pass filter cutoff frequency." (emphasis

added). *See*, Specification, page 4, lines 3-5. Apparently, the Examiner inadvertently missed the point that any reduction in the shunt capacitance of the ESD clamp is for low frequency signals (frequencies below the low pass filter cut-off frequency). Basically, this passage provides for a low pass filter. This is in direct contradiction to ***Kleveland's*** disclosure, which allows high frequency signals to pass (*i.e.*, a high pass filter). Therefore, ***Kleveland*** discloses the opposite of a low pass filter. Hence, ***Kleveland*** clearly does not anticipate all of the elements of claims 1 and 21 of the present invention.

In the Final Office Action dated December 3, 2004, the Examiner asserted that Appellants argued that ***Kleveland*** is directed to reducing parasitic capacitance of the protection circuit to reduce data transmission in high frequency devices and, therefore, does not function as a low pass filter. The Examiner disagreed with this argument. *See*, *Response to Argument* section in the Final Office Action dated December 3, 2004. Firstly, Appellants respectfully assert that the Examiner inadvertently mischaracterized Appellants' argument (Appellants' arguments are described below). Secondly, ***Kleveland*** affirmatively asserts that the circuitry disclosed is not a low pass filter, but calls for high performance required by high frequency applications. *See* col. 5, lines 22-26. ***Kleveland*** clearly asserts that at low frequencies, the circuit is protected from ESD discharge events, at the same time, the ESD protection circuit provides high performance required by high frequency applications. Further, ***Kleveland*** expressly asserts that for high frequency signals, its ESD circuit performs like a transmission line. *See* col. 5, lines 21-22. Therefore, ***Kleveland*** expressly discloses that its system is not a low pass filter.

In contrast to ***Kleveland***, claim 1 in the present invention calls for forming a low pass filter. ***Kleveland*** indeed teaches the opposite subject matter as compared to the elements called for by claim 1 of the present invention. Additionally, Appellants had argued that ***Kleveland*** is directed towards reducing capacitance of ESD protection and promoting a reduction of the parasitic capacitance in an attempt to avoid reducing the bandwidth of high frequency devices. In contrast to disclosure in ***Kleveland***, claim 1 calls for the ESD devices being connected to a plurality of turns of an inductor, where the inductor and the parasitic capacitance of the ESD device are used to form a low pass filter. In other words, for high frequency signals, the parasitic capacitance of the ESD device of the present invention is useful in performing a low pass filtering process. Therefore, ***Kleveland*** performs the opposite of the claimed elements. Upon an examination of ***Kleveland***, those skilled in the art would be directed away from the claims of the present invention. ***Kleveland*** discloses attempting to reduce or eliminate parasitic capacitance, wherein claims of the present invention call for using the inductance of the turns, in combination with the parasitic capacitance to form a low pass filter. Therefore, ***Kleveland*** does not disclose all of the elements of the claimed invention. In addition, ***Kleveland*** actually teaches away from the claims of the present invention.

In the Final Office Action dated December 3, 2004, the Examiner asserted that Appellants' disclosure admits that all ESD devices include significant amount of parasitic capacitance that may degrade high frequency signals. Firstly, Appellants' disclosure did not disclose that all ESD includes significant parasitic capacitance, it merely asserted that "these" ESD devices have parasitic capacitance. However, Appellants respectfully assert that this assertion is of no consequence because the issue is not whether all ESD devices include a

significant amount of parasites. As described above, parasitic capacitance is being used in a novel manner to form a low pass filter, as called for in claims 1 and 21, which is not disclosed by ***Kleveland***.

Also in the Final Office Action dated December 3, 2004, the Examiner asserted that ***Kleveland*** provided the structure that is identical to claims 1-3. In the Final Office Action dated December 3, 2004, the Examiner asserted that ***Kleveland*** discloses an inductor being connected to the ESD device in a low pass filter configuration using the capacitances of the ESD devices. *See* page 5, Final Office Action dated December 3, 2004. Appellants respectfully disagree with Examiner's assertion. Examiner cites col. 3, lines 56-58 and col. 5, lines 21-30 of ***Kleveland*** to support this assertion. However, Appellants assert that neither of these citations, or any other passages in ***Kleveland***, support such an assertion. For example, in col. 3, lines 55-58, ***Kleveland*** discloses that the capacitance of the ESD device can be part of the transmission line and it minimally degrades the bandwidths of the signal. This disclosure in ***Kleveland*** implies that a low pass filter is not formed, in contrast to the element of claim 1, which calls for the formation of a low pass filter. In fact, ***Kleveland*** attempts to only minimally degrade the bandwidth of high frequency and low frequency transmission, which is clearly not a definition of a low pass filter.

Additionally, the other passage cited by the Examiner (col. 5, lines 21-30 of ***Kleveland***) discloses that for high frequency signals, the ESD protection device behaves like a transmission line. Therefore, it is perfectly clear that the disclosure of ***Kleveland*** does not seek to prevent high frequency transmissions; in fact, it clearly states that the ESD protection 240 of ***Kleveland*** performs like a transmission line during high frequency transmission. This is opposite of what is called for by claims 1 and 21 of the present invention, which call for a low pass filter, thereby

substantially restricting high frequency signals. Therefore, Examiner's assertion that ***Kleveland*** provides identical structure, as set forth in claims 1-3, as argued in the Final Office Action dated December 3, 2004, is unfounded and not supported by the disclosure of ***Kleveland***. In fact, the disclosure of ***Kleveland*** clearly supports the opposite assertion and ***Kleveland*** does not disclose elements called for by claim 1 of the present invention, including the element of forming the low pass filter. Therefore, ***Kleveland*** does not anticipate all of the elements of the claims of the present invention. Additionally, Appellants respectfully assert that ***Ling*** does not add disclosure to make up for the missing elements of claims 1 and 21 that is not taught by ***Kleveland***. In fact, since ***Kleveland*** teaches away from the elements of the claims of the present invention, simply combining ***Ling*** would not make obvious all of the elements of the present invention. These arguments are discussed in more details below. Therefore, claims 1 and 21 of the present invention are not taught, disclosed, or suggested by the cited prior art and, thereby, are allowable.

As described above, ***Kleveland*** does not teach, disclose, or suggest all of the elements of claims 1 and 21 of the present invention. ***Kleveland*** actually directs one away from the present invention. ***Kleveland*** is directed towards reducing parasitic capacitance of ESD protection circuits. *See* col. 1, lines 35-38. ***Kleveland*** promotes reducing parasitic capacitance in an attempt to avoid reducing the bandwidth of high frequency devices. *See* col. 2, lines 5-8. ***Kleveland*** is directed to attempt reducing or eliminating the parasitic capacitance to reduce data transmission errors. In contrast to ***Kleveland***, claims 1 and 21 of the present invention call for a plurality of ESD clamp devices being connected to a corresponding one of a plurality of turns on an inductor, wherein the inductor and the parasitic capacitance is used to form a low pass filter.

Additionally, ***Kleveland*** does not mention the utilization of parasitic capacitance. ***Kleveland*** merely mentions the undesirability of parasitic capacitance, wherein claims of the present invention utilize turns of an inductor in conjunction with the parasitic capacitance of the ESD clamp devices to form a low pass filter. Therefore, ***Kleveland*** does not teach these elements of claims 1 and 21.

Furthermore, claims 1 and 21 also call for an inductor coil for generating an inductance for the low pass filter. The disclosure in ***Kleveland*** does not disclose the plurality of ESD clamp devices with the parasitic capacitance being connected to corresponding turns of an inductor to form a low pass filter. In fact, ***Kleveland*** directs one away from the parasitic capacitance and, therefore, does not disclose the low-pass filter elements called for by claim 1 of the present invention. Therefore, claims 1 and 21 of the present invention are allowable. Accordingly, Appellants respectfully assert that the Examiner erred in maintaining the rejection of Group I claims (claims 1-3 and 21-24) under 35 U.S.C. § 102(a) because the Examiner did not meet the legal standards to establish anticipation based upon ***Kleveland***. Therefore, claims 1-3 and 21-24 are allowable.

Independent claims 1 and 21 are allowable for at least the reasons cited above. Additionally, dependent claims 2-3, and 22-24, which respectively depend from independent claims 1 and 21, are also allowable for at least the reasons cited above.

B. Claims 4-20 Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by U.S. Patent No. 5,969,929 (*Kleveland*) in view of U.S. Patent No. 5,576,680 (*Ling*).

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to the alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Health-care Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior

art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success viewed in light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991; *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

Appellants respectfully assert that the Examiner did not meet the legal standards to reject the claims of the present invention under 35 U.S.C. § 103(a) because the prior art references (***Kleveland*** and ***Ling***) do not teach or suggest all of the claim limitations of the claims of the present invention. Additionally, the Examiner has not provided sufficient evidence or arguments that there is a suggestion that one skilled in the art would have been motivated to combine the references (***Kleveland*** and ***Ling***). In fact, Appellants provide arguments that ***Kleveland*** and ***Ling*** would not have been combined by one skilled in the art. Therefore, the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness under 35 U.S.C. § 103(a) with regards to claims 4-20 of the present invention.

Group II Claims (Claims 4, 9, and 14-20) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Kleveland* in view of *Ling*. Group II claims stand or fall together.

Group II claims are generally directed to a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter. Group II claims are also directed to a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter. In contrast, ***Kleveland*** is directed to reducing capacitance of ESD protection and providing a reduction in the parasitic capacitance in order to maintain the bandwidth of high frequency devices. Therefore, the disclosure of

Kleveland provides for passing high frequency signals, which is in stark contrast with Group II claims. Additionally, the disclosure of ***Ling*** does not compensate for the deficit of ***Kleveland***. For example, ***Ling*** does not disclose ESD protection or utilization of parasitic capacitance with inductor turns to make up for the deficit of ***Kleveland***. ***Ling*** is directed to forming an inductive circuit on a semiconductor chip, however, ***Ling*** does not disclose the subject matter that is lacking in ***Kleveland,*** but called for by claims of the present invention.

Contrary to the Examiner's assertions in the Final Office Action dated December 4, 2004, Applicants respectfully assert that ***Ling*** does not disclose that a via could be used to connect coil shaped elements to produce an inductive element, as called for by claim 4 of the present invention. ***Ling*** discloses a via to connect an inductive core to conductive lines, not connecting coil turns on different layers. *See*, col. 4, lines 39-49. Therefore, ***Ling*** does not provide the subject matter that the Examiner uses to combine with ***Kleveland*** in order to make obvious independent claims 4 and 18.

In the Final Office Action dated December 4, 2004, the Examiner stated that ***Kleveland*** does not disclose that each of the turns of the inductor are formed from a separate layer of the integrated circuit. The Examiner then provides the disclosure of ***Ling*** to provide the inductive circuit 400 by connecting a plurality of inductor coils having a plurality of turns formed from different horizontal planes of the IC chip. *See* col. 7, lines 59-col. 8, line 7. However, Applicants respectfully assert that the addition of ***Ling*** does not make up for the deficits of ***Kleveland***. One reason is because ***Kleveland*** does not disclose the use of the parasitic capacitances provided by the plurality of ESD clamp devices being coupled to corresponding turns of an inductor to form a low pass filter. ***Ling*** does not provide this disclosure; therefore,

the mere addition of ***Ling*** does not make up for the deficit of ***Kleveland***. Also, ***Ling*** does not disclose the element that the Examiner claims is missing from ***Kleveland***, e.g., a via used to connect coil shaped inductive elements to produce an inductive element, as called for by in claim 4 of the present invention.

Further, ***Ling*** simply does not disclose ESD protection or utilization of parasitic capacitance with inductor turns to make up for the deficit of ***Kleveland***. ***Ling*** is merely directed to forming an inductive circuit on a semiconductor chip. ***Ling*** provides for patterned lines to form an inductor. Although ***Ling*** discloses a plurality of inductor elements formed on different horizontal planes, ***Ling*** does not disclose the subject matter that is lacking in ***Kleveland,*** but called for by claims of the present invention. *See* col. 7, lines 59-65. Therefore, combining ***Kleveland*** and ***Ling*** would still not disclose the elements of utilizing a plurality of ESD clamp devices with a parasitic capacitance being connected to corresponding turns of an inductor in order to provide a low pass filter, as called for by claim 4 of the present invention. Therefore, claims 3-17, which directly or indirectly depend from claim 4, are not taught, disclosed, or made obvious by ***Kleveland***, ***Ling***, or their combination. Additionally, claim 18, which provides a method for forming a plurality of conductive layers provides ESD clamp devices, which are then connected to corresponding coil turns to form a low pass filter for at least the reasons described above. Therefore, claim 18 of the present invention is allowable. Additionally, claims 19 and 20, which depend from claim 18 are also allowable for similar reasons cited above. Furthermore, previously added claim 21, which calls for a device comprising a plurality of ESD clamp devices with a parasitic capacitance being connected to corresponding turns of an inductor, in order to

provide a low pass filter, is also not taught or made obvious by ***Kleveland***, ***Ling***, or their combination, for at least the reasons cited above.

Furthermore, contrary to the Examiner's assertions in the Final Office Action dated December 4, 2004, Appellants respectfully assert that one skilled in the art would not combine ***Kleveland*** and ***Ling*** to make obvious all of the claims of the present invention. ***Kleveland*** is directed to distributed ESD protection in a device, wherein ***Ling*** is directed to forming an inductor on a substrate using line patterns and an inductive core. Without improper hindsight, one skilled in the art would not combine the teaching of ***Kleveland*** and ***Ling*** to make obvious all of the claims of the present invention. Contrary to the Examiner's assertions in the Final Office Action dated December 4, 2004, Appellants assert that, without gleaning only from Appellants' disclosure, a reconstruction of elements of the claimed invention would not be possible. There is no indication in either prior art (***Kleveland*** or ***Ling***) that a via could be used to connect coil shaped elements to produce an inductive element, as described in the Specification and claimed in claim 4 of the present invention. *See* pages 10-11 of the Specification. ***Ling*** discloses a via to connect an inductive core to conductive lines, not connecting inductive coils on different layers. *See*, col. 4, lines 39-49 of ***Ling***. Therefore, one skilled in the art would not be motivated to combine ***Ling*** with ***Kleveland*** to make obvious all of the elements of the present invention. Hence, one would need improper hindsight by gleaning only from Appellants' disclosure to make obvious all of the elements of the claims of the present invention. However, *arguendo*, even if ***Kleveland*** and ***Ling*** were combined, all of the elements of the claims of the present invention would not be obvious to those skilled in the art as described above. Additionally, independent claims 18 and 21 are also not made obvious by ***Kleveland***, ***Ling*** or their

combination for at least the reasons described above. Accordingly, Appellants respectfully assert that the Examiner erred in maintaining the rejection of Group II claims (claims 4, 9, and 14-20) under 35 U.S.C. § 103(a) because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Kleveland***, ***Ling***, or their combination. Therefore, claims 4, 9, and 14-20 are allowable.

Independent claims 4, 18, and 21 are allowable for at least the reasons cited above. Additionally, dependent claims 5-17, 19-20, and 22-24, which respectively depend from independent claims 4, 18, and 21, are also allowable for at least the reasons cited above.

Group III Claim (Claim 10) Is Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Kleveland* in view of *Ling*. Group III claim stands or falls by itself.

As described above, ***Kleveland***, ***Ling***, or their combination, do not disclose or make obvious a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter, which are elements of claim 4, from which Group III claim (*i.e.*, claim 10) indirectly depends. ***Kleveland***, ***Ling***, or their combination, also do not disclose a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter, which are elements of claim 4, from which claim 10 indirectly depends. Therefore, claim 10 is not anticipated or made obvious by ***Kleveland***, ***Ling***, or their combination.

Additionally, Group III claim (*i.e.*, claim 10) also calls for the conductive layer being made from metal, which is selected from the group consisting of copper, aluminum, copper alloy and aluminum alloy. There is no disclosure in ***Kleveland***, ***Ling***, or their combination that

provides for the novel formation of conductive layers, as well as the conductive layers being made from a metal, which is selected from a group consisting of copper, aluminum, copper alloy and aluminum alloy. ***Kleveland***, ***Ling***, or their combination do not anticipate or make obvious such subject matter. Therefore, Group III claim (claim 10) is allowable for at least the reasons cited herein. Accordingly, Appellants respectfully assert that the Examiner erred in maintaining the rejection of Group III claim (claim 10) under 35 U.S.C. § 103(a) because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Kleveland***, ***Ling***, or their combination. Therefore, claim 10 is allowable.

Group IV Claims (Claims 12 and 13) Are Not Rendered Unpatentable under 35 U.S.C. § 103(a) by *Kleveland* in view of *Ling*. Group IV claims stand or fall together.

As described above, ***Kleveland***, ***Ling***, or their combination, do not disclose or make obvious a plurality of conductive layers forming coil turns and being connected using vias through an interleaved insulation layer to form an inductor coil for a low pass filter, which are elements of claim 4, from which Group IV claims (*i.e.*, claims 12 and 13) depend. ***Kleveland***, ***Ling***, or their combination also do not disclose a plurality of ESD clamp devices having parasitic capacitances to help form a low pass filter, which are elements of claim 4, from which claims 12 and 13 depends. Therefore, claims 12 and 13 are not anticipated or made obvious by ***Kleveland***, ***Ling***, or their combination.

Additionally, claim 12 calls for a magnetic material that is provided concentrically inside of an inner diameter of the coil turns of the plurality of conductive layers. This provides for an increase of the inductance thereof. The use of the concentrically positioned magnetic material to

increase the inductance is not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. No subject matter to this effect is provided neither in ***Kleveland*** nor in ***Ling***. Therefore, all of the elements of claim 12 are not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. Accordingly, claim 12 is allowable for at least the reasons cited herein.

Furthermore, claim 13, which depends from claim 12, provides the additional element of the magnetic material being of a material that is selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide. As described above, ***Kleveland***, ***Ling***, or their combination do not disclose or make obvious the magnetic material called for by claim 13. Additionally, ***Kleveland***, ***Ling***, or their combination also do not disclose the use of the material selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide for the magenetic material. Therefore, all of the elements of claim 13 are not disclosed or made obvious by ***Kleveland***, ***Ling***, or their combination. Accordingly, claim 13 is allowable for at least the reasons cited herein. For at least the reasons cited above, claims 12 and 13 of the present invention are allowable. Accordingly, Appellants respectfully assert that the Examiner erred in maintaining the rejection of Group IV claims (claims 12 and 13) under 35 U.S.C. § 103(a) because the Examiner did not meet the legal standards to establish a *prima facie* case for obviousness based upon ***Kleveland***, ***Ling***, or their combination. Therefore, claims 12 and 13 are allowable.

CONCLUSION

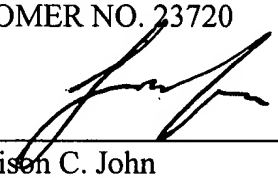
In view of the foregoing remarks, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-24, over the prior art of

record. In view of the foregoing, Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the decision rejecting claims 1-20 and direct the Examiner to pass the case to issue. **The undersigned attorney may be contacted at (713) 934-4069** with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

WILLIAMS, MORGAN & AMERSON, P.C.
CUSTOMER NO. 23720

Date: June 1, 2005

By: 

Jaison C. John
Reg. No. 50,737
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)
ATTORNEY FOR APPELLANTS

APPENDIX A

1. (Previously presented) An electrostatic discharge (ESD) protection network, comprising:

an inductor having a plurality of turns in the shape of a coil, the plurality of turns having an inductance;

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of said plurality of turns of said inductor, the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter and;

at least one via for forming an inductor coil for generating an inductance for said low pass filter.

2. (Previously presented) The ESD protection network of claim 1, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on a surface selected from the group consisting of a substrate and an integrated circuit die.

3. (Previously presented) The ESD protection network of claim 1, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on an integrated circuit die.

4. (Previously presented) An integrated circuit apparatus having an electrostatic discharge (ESD) protection network, said apparatus comprising:

an integrated circuit substrate;

a first insulation layer over a face of said integrated circuit substrate;

a plurality of conductive layers, each of the plurality of conductive layers in the shape of a coil turn, the coil turn having a first and second end;

a plurality of insulation layers interleaved between the plurality of conductive layers;

a one of said plurality of conductive layers proximate to said first insulation layer and the other ones of said plurality of conductive layers stacked over the one with said plurality of insulation layers interleaved therebetween;

a plurality of vias in the plurality of insulation layers, the plurality of vias connecting adjacent ones of the coil turns of said plurality of conductive layers, thereby forming an inductor coil for generating an inductance for said low pass filter; and

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of the coil turns of said plurality of conductive layers, thereby forming a low pass filter.

5. (Original) The apparatus of claim 4, wherein respective ones of said plurality of conductive vias connect the second ends of each one of the coil turns of said plurality of conductive layers to the first ends of each of the adjacent ones of the coil turns of said plurality of conductive layers, thereby forming the inductor coil.

6. (Original) The apparatus of claim 5, wherein each of the respective ones of said plurality of conductive vias is at least one via.

7. (Original) The apparatus of claim 5, wherein each of the respective ones of said plurality of conductive vias is two or more vias so as to reduce electrical connection resistance thereof.

8. (Original) The apparatus of claim 4, wherein the shape of the coil turns of said plurality of conductive layers is selected from the group consisting of round, square, rectangle, triangle, oval, hexagon and octagon.

9. (Original) The apparatus of claim 4, wherein said plurality of conductive layers is made of metal.

10. (Original) The apparatus of claim 9, wherein the metal is selected from the group consisting of copper, aluminum, copper alloy and aluminum alloy.

11. (Original) The apparatus of claim 1, wherein said plurality of conductive layers is made of conductive doped polysilicon.

12. (Original) The apparatus of claim 4, further comprising a magnetic material interposed concentrically inside of an inner diameter of the coil turns of said plurality of conductive layers so as to increase the inductance thereof.

13. (Original) The apparatus of claim 12, wherein the magnetic material is selected from the group consisting of iron, iron oxide, ferrite ceramic and ferrous oxide.

14. (Original) The apparatus of claim 4, wherein at least one ESD claim device is connected to each one of said plurality of conductive layers.

15. (Original) The apparatus of claim 4, wherein at least one of said plurality of conductive layers is connected to a one of said plurality of ESD claim devices.

16. (Original) The apparatus of claim 4, wherein said plurality of ESD clamp devices are fabricated in said integrated circuit substrate and connected to said plurality of conductive layers with vias through said plurality of insulation layers.

17. (Original) The apparatus of claim 4, wherein said plurality of ESD claim devices are fabricated on at least one of said plurality of insulation layers and connected to said plurality of conductive layers with vias through said plurality of insulation layers.

18. (Previously presented) A method for providing an electrostatic discharge (ESD) protection network, comprising:

forming a plurality of conductive layers and a plurality of insulation layers, wherein said plurality of conductive layers and said plurality of insulation layers are interleaved, wherein each of the conductive layers is formed in the shape of a coil

turn having an inductance such that such that each of the coil turns has a first and a second end;

forming a plurality of vias in said plurality of insulation layers, the plurality of vias being located between the ends of adjacent coil turns wherein conductive material is formed in said plurality of vias thereby connecting the first end of one coil turn to the second end of the adjacent coil turn for generating an inductance for said low pass filter;

providing a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance; and

connecting said plurality of ESD clamp devices to a corresponding one of the coil turns of said plurality of conductive layers, thereby forming a low pass filter.

19. (Original) The method of claim 18, wherein the step of connecting said plurality of ESD clamp device comprises the step of connecting at least one ESD clamp device to each one of said plurality of conductive layers.

20. (Original) The method of claim 18, wherein the step of connecting said plurality of ESD clamp devices comprises the step of connecting at least one of said plurality of conductive layers is to a one of said plurality of ESD clamp devices.

21. (Previously Presented) A device comprising a protection circuit, said protection circuit comprising:

an inductor having a plurality of turns in the shape of a coil, the plurality of turns having an inductance;

a plurality of electrostatic discharge (ESD) clamp devices, each one of said plurality of ESD clamp devices having a parasitic capacitance, said plurality of ESD clamp devices being connected to a corresponding one of said plurality of turns of said inductor, the inductance of said turns and the parasitic capacitance of said ESD clamp devices thereby forming a low pass filter and;

at least one via for forming an inductor coil for generating an inductance for said low pass_filter.

22. (Previously Presented) The device of claim 21, wherein said device is a semiconductor device.

23. (Previously Presented) The device of claim 21, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on a surface selected from the group consisting of a substrate and an integrated circuit die.

24. (Previously Presented) The device of claim 21, wherein said plurality of turns and said plurality of ESD clamp devices are fabricated on an integrated circuit die.